REMARKS

Claims 1-3 and 9-18 are presently active, claims 4-8, 19, and 20 having been cancelled without prejudice by this Amendment.

In the Office Action dated 23 January 2004 ("Office Action"), claims 1-20 were rejected under 35 U.S.C. §102(b) as being anticipated by Smith, U.S. patent 4,992,674 ("Smith").

An informality is corrected in the specification of the present application. The specification as originally filed used the label "108" to refer both to the interface and the physical medium in Fig. 1. Accordingly, the specification is corrected by referring to the physical medium as "109", and a corrected Fig. 1 is provided to amend the drawings.

To better define the invention, claims 1, 9, and 17 are amended. These are all of the currently active independent claims. Dependent claims 2 and 3 are amended to also better define the invention. As discussed below, Applicants believe that independent claims 1, 9, and 17 are not anticipated by Smith.

Claim 1 includes the following two limitations: (1) a transistor to discharge the capacitor for a discharge time interval by conducting a transistor conduction current, where the transistor is coupled to the capacitor so that the capacitor has a discharge current substantially equal to the transistor conduction current during a first portion of the discharge time interval; and (2) a second current source coupled to the transistor and the capacitor so that for a second portion of the discharge time interval the capacitor has a discharge current less than the transistor conduction current.

Now refer to Fig. 1 of Smith. Because the gates of transistors 14 and 16 are connected to the output of comparator 12, either transistor 14 is ON so that current source 18 charges capacitor 22, or transistor 16 is ON so that current source 20 discharges capacitor 22. Transistors 16 and 14 cannot both be ON. So, during the "discharge interval" when capacitor 22 is discharging through transistor 16, all of the current being discharged from capacitor 22 flows through transistor 16. But there is no second current source coupled to the capacitor such that the discharge current from the capacitor is less than the transistor conduction current through transistor 16 during a second portion of the discharge time interval. Note that transistor 14 is OFF when capacitor 22 is discharging

through transistor 16, and that the discharge current from capacitor 22 is equal to the transistor conduction current through transistor 16. Therefore, the claim limitation labeled (2) in the previous paragraph is not present in Fig. 1, and consequently claim 1 is not anticipated by Smith.

Claim 9 recites the limitation of "a transistor having a drain and having a gate connected to the node". Note that neither transistor 14 nor 16 in Fig. 1 of Smith has its gate connected to the "node", which in this case is the non-grounded terminal of capacitor 22. Therefore, claim 9 is not anticipated by Smith.

Claim 17 recites the limitations: (1) a FET to discharge the capacitor for a discharge time interval by conducting a drain current, the FET having a gate connected to the node during the discharge time interval; and (2) a second current source coupled to the node during a portion of the discharge time interval so that the capacitor has a discharge current less in magnitude than the drain current. Again, neither transistor 14 nor transistor 16 in Fig. 1 of Smith has its gate connected to the node. And furthermore, there is no second current source so that the capacitor has a discharge current less in magnitude than the drain current of transistor 16 when discharging (or transistor 14 when charging). Consequently, claim 17 is not anticipated by Smith.

Accordingly, because all of the presently active independent claims are not anticipated by Smith, Applicants believe that all of the presently active claims are patentable over Smith.

Respectfully submitted,

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Annotated Sheet Showing Changes

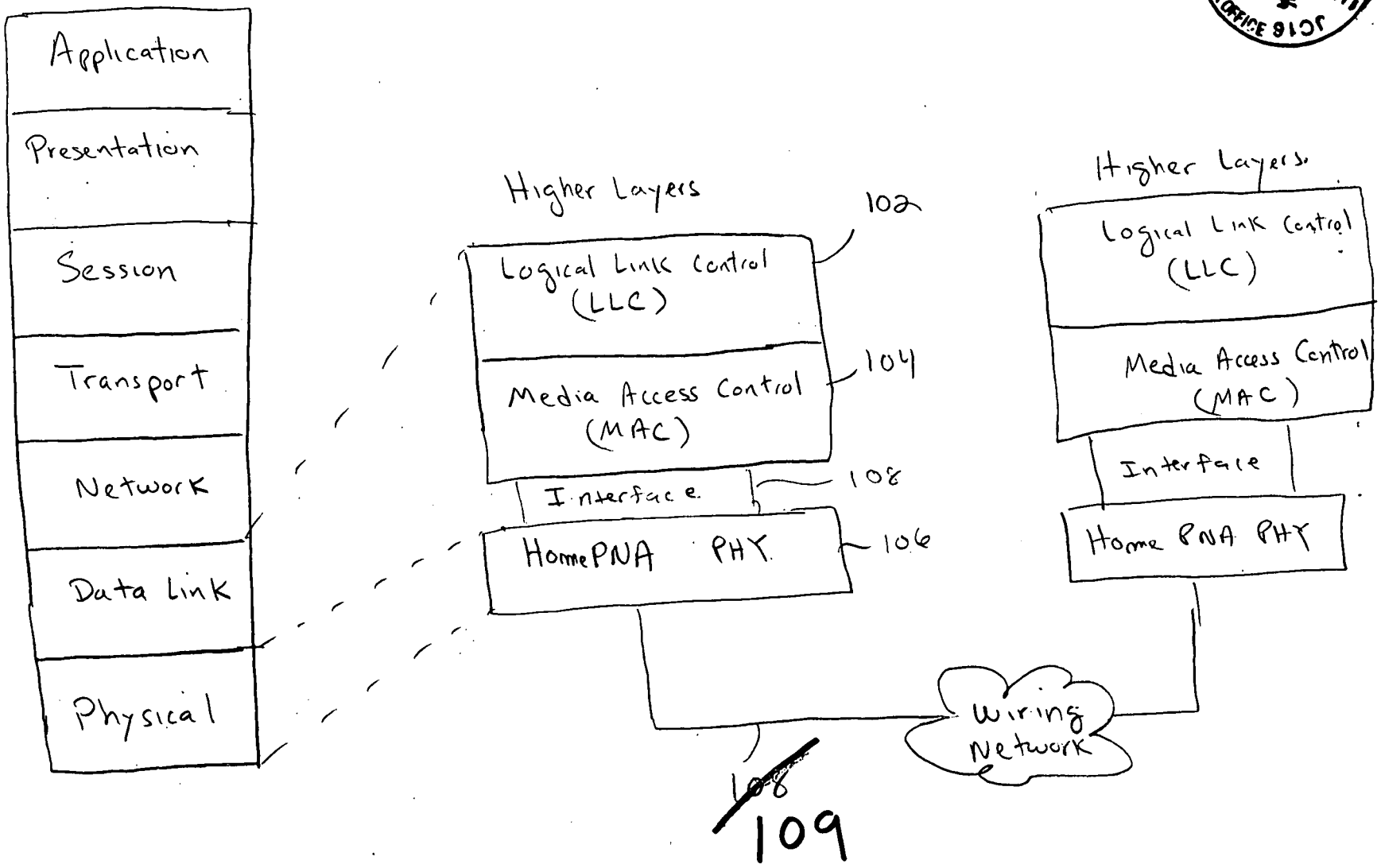

Fig. 1 (Prior Art)